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A WIDE TUNING RANGE, LOW VOLTAGE CMOS RING OSCILLATOR

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ABSTRACT

This paper presents a wide tuning range voltage controlled ring oscillator (VCO) with a frequency range of 3.2 to 8.0 GHz. The proposed design is simulated using 0.13 μ m CMOS technology with a supply headroom of 1.2V. A programmable current switching technique is introduced to select between different tuning curves, which helps in reducing the VCO gain and results in improving the phase noise performance.

The aim of this research was to study the limitations of a ring based oscillators in the appreciation of high frequency operation along in achieving wide tuning range in low voltage CMOS process. Different VCO topologies have been mentioned in [1]-[5] to demonstrate wide tuning range and high oscillation frequency. [1] and [2] adopts large supply headroom of 1.6V and 1.8V exhibiting a single tuning curve encapsulating the depicted frequency range of operation, which results in large VCO gain. The reported designs are more sensitive to noise and cause large variations across tuning range, which is not desirable for the practical integration of phase locked loop (PLL) circuitry.

A dual delay path technique is used in [3] and [4] to increase the oscillation frequency. The exact topology is used in [5] to improve the tuning range by adding switched capacitors. This design works in a top down topology, where the frequency curve can be shifted to a lower one by enabling more capacitance. Dividing the tuning range into multiple curves helps in reducing the VCO gain and improves the phase noise, however this topology suffers with a limitations on voltage swing and lags in large tuning range. It is observed that, adding more capacitance at the output of a delay cell results in the reduction of voltage swing and also limits the frequency range of operation.

An enhanced approach is presented in this work in achieving wide range of frequency operation for a ring oscillator solution. Instead of adding capacitors, a programmable current source is integrated in parallel to the regular tail current source. A bottom up topology is used to divide the whole tuning range into multiple tuning curves as in Figure 1. The frequency for a certain tuning curve is controlled by varying the tuning voltage up to 1.2V as the range can be switched to higher tuning curve by selecting the programmable current. The tuning range coverage is divided into 10 curves depicted from T1 to T10 as in Figure 1, while the current for each curve is controlled via programming current ranging from 0 to 4mA in step interval of 400uA. This helps in sustaining the rail to rail swing and provides a lower VCO gain across all the curves.

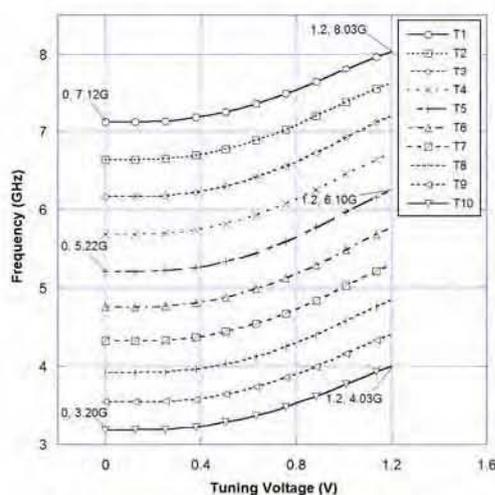


Figure 1. Proposed VCO frequency tuning range

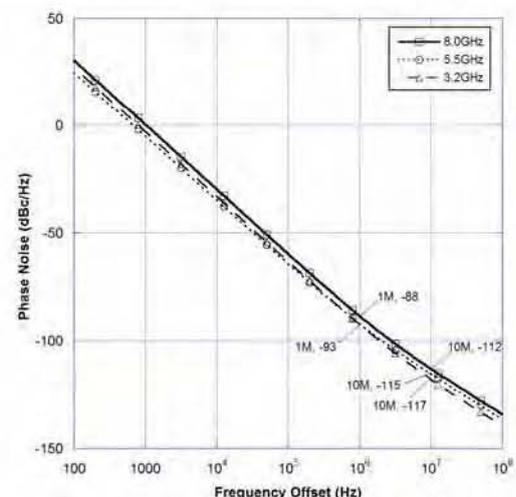


Figure 2. Phase Noise at 3.2, 5.5 and 8.0GHz

Simulation results shows promising VCO performance along with a wide tuning range output. The VCO tuning range as shown in Figure 1 encapsulates a frequency range of 3.2 to 8.0 GHz. The VCO integrated with the programming current source consumes a maximum current of 10mA. Phase noise simulation shows acceptable noise performance at 3.2, 5.5 and 8.0 GHz with a value of -93, -93 and -88 dBc/Hz at 1MHz offset, while achieving -112, -115 and -117 dBc/Hz at 10MHz offset. The proposed design has a lower VCO gain along with an ability to further increase the tuning range without affecting the VCO performance. VCO can be used for different applications in ultra-wideband (UWB) frequency range.

Keywords: CMOS, phase noise, programmable current source, phase noise, VCO, wide tuning range.

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